TRUETIME

Model 560-5201-X
Fiber Optic FM Transceiver Manual

SECTION ONE

1. GENERAL INFORMATION

1.1. PURPOSE OF EQUIPMENT

The Model 560-5201-X Fiber Optic FM Transceiver card provides a single fiber optic input interface for the backplane bus IN[1:8]. The input interface signals are re-transmitted for repeater mode (ECHO) operation. The card can be configured to drive any 1 signal line of the IN[1:8] backplane bus. The card is intended to be configured as a repeater only and no provisions have been made for independent output operation. This assembly provides CW mode fiber communications.

The IN[1:8] backplane signals are distributed via 50 ohm controlled-impedance traces, terminated at Slot 17. For best signal quality, the Transceiver card should be located in Slots 1 through 4.

1.1.1. PHYSICAL SPECIFICATIONS

Dimensions:	0.8” W x 4.4” H x 5.0” D (2 cm x 11 cm x 13 cm)
Weight:	Approximately ½ pound (¼ kg)

1.1.2. ENVIRONMENTAL SPECIFICATIONS

Operating Temp:	0° to +50°C
Storage Temp:	-17° to +100°C
Humidity:	Up to 95% relative, non-condensing
Cooling Mode:	Convection

1.1.3. POWER REQUIREMENTS

Voltage:	48 VDC ±20%
Power:	3 W

1.1.4. FUNCTIONAL SPECIFICATIONS

1.1.4.1. RECEIVER FIBER OPTIC INPUT

Signal:	890 nM, -16 dBm to -26 dBm
Connector:	ST
Fiber Type:	Multi-mode 50, 62.5 or 100 micron

1.1.4.2. TRANSMITTER FIBER OPTIC OUTPUT

Signal:	890 nM, -18.8 dBm typical, into 50 micron fiber
Signal:	890 nM, -16 dBm typical, into 62.5 micron fiber
Signal:	890 nM, -12 dBm typical, into 100 micron fiber
Connector:	ST

1.1.4.3. RECEIVER BACKPLANE INPUT TO IN

560-5201-1	Signal Type:	Sinewave, DC-coupled
	Amplitude:	2-4 Vp-p into 50 ohms
560-5201-2	Signal Type:	Squarewave, DC-coupled
	Amplitude:	2-4 Vp-p into 50 ohms

1.1.4.4. DRC CARD COMPATIBILITY

Location:	Slots 1-4
Compatibility:	See DRC Card Compatibility Matrix

SECTION TWO

2. INSTALLATION AND OPERATION

2.1. HOT-SWAPPING

All cards, input cables and output cables are hot swappable. It is not necessary to remove chassis power during insertion or removal. Hot swapping and reference-source changes are abrupt, the effects difficult to characterize; however, the system is designed to protect against permanent effects and minimize temporary effects of these events.

Typically, adjacent-card hot swapping has a negligible effect on the Fiber Optic Transceiver. The hot swapping event typically lasts less than one clock-period and has an average of 0 Volts. The effect of redundant power supply switch-over is also negligible.

Hot swapping of a Fiber Optic Transceiver affects the system in varying ways depending upon whether it is configured to drive IN1 to IN8 and depending upon which reference input is the currently-highest priority. These effects are discussed in individual card manuals.

2.2. REMOVAL AND INSTALLATION

CAUTION: Individual components on this card are sensitive to static discharge. Use proper static discharge procedures during removal and installation.

Refer to CARD COMPATIBILITY section prior to installing new card.

To remove card, loosen the captive retaining hardware at the top and bottom of the assembly, then firmly pull on the handle (or on any connector on rear panel adapter cards) at the bottom of the card. Slide the card free of the frame. Refer to the SETUP section for any required switch settings; or set them identically to the card being replaced. Reinstall the card in the frame by fitting it into the card guides at the top and bottom of the frame and sliding it in slowly, avoiding contact between bottom side of card and adjacent card front panel, until it mates with the connector. Seat card firmly to avoid contact bounce. Secure the retaining screws at the top and bottom of the card assembly.

2.3. SETUP

The setup of the Fiber Optic Transceiver involves selection of the timing bus line: IN1 through IN8 and whether the signal applied to the bus is to be AC or DC. Refer to the tables below. Please note that the switch position number of SW2 does not always correspond to the timing bus number.

Mode Select Jumper JP1

MODE OF OPERATION/	ANALOG (560-5201-1)	DIGITAL (560-5201-2)
JUMPER POSITION	JP1-1 TO JP1-2	JP1-2 TO JP1-3

Input Buss Select SW1

Reserved for future use.

Input Buss Select SW2

INPUT BUS/ SWITCH POSITION	IN1	IN2	IN3	IN4	IN5	IN6	IN7	IN8
SW2-1	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
SW2-2	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
SW2-3	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
SW2-4	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
SW2-5	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
SW2-6	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
SW2-7	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
SW2-8	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON

2.4. FAULT INDICATION

This card has the Configuration Fault LED D5 and two Fault Status bits which are reported to the Fault Monitor CPU.

2.4.1. INIT. FAULT INDICATOR

This is an on-card fault indicator which is not externally visible; although it can be seen by installing the card next to an empty slot. It indicates a failure of the card to initialize properly during power-up. Occasionally, this fault is caused by a temporary condition related to the cycling of power and can be cleared by a power or hot swap cycle. If this is unsuccessful, the card is defective.

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2.4.4 DETAILED FAULT STATUS VIA CPU

The Fault Monitor CPU has access to 560-5201 card fiber and copper bus signal status. The Verbose report displays the Fault status. In this context, a reported fault indicates a problem. The Machine report, when used, reports the current status (settings) of the switches and faults in hexadecimal characters. Together, they pinpoint problems and help the technician view the switch settings on the cards.

This status is available via the Fault Monitor CPU serial port. Individual bit definitions are as follows:

Spare	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Bus Fault***	**Fiber Driver Fault***
8	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**	**8**	**4**	**2**	**1**
2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
0	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*0*	*1*	*0*
High Byte High Nibble				High Byte Low Nibble				Low Byte High Nibble				Low Byte Low Nibble			
0				**0**				**0**				**2**			

Fault Status F1 Report

Fault Status F0 Report

Key:

* Latched Fault Bit -- Reset Via Fault Monitor CPU.

Above each 8,4,2,1 is the corresponding fault for that bit. For instance, above the 8 bit in the Upper byte/Low nibble reads " Spare". In the above example, the report reads 0002. A two in binary is 1,0. From right to left, the 0 is in the Lower byte/low nibble under Hex weight 1. The fault (indicated by a 1) is under Hex weight 2. If there had been a fault (indicated by a 1) under Hex weight 1, the total hex weight is 3 (2+1).

Shaded area
Informational only. The upper row: Bit value hex weights (8,4,2,1) The Lower row corresponds to the hex weight above. For instance, a 7 is 111 in binary.

Each section of 8,4,2,1 is a nibble of either an Upper or Lower byte and separated for easy recognition. Each nibble = 4 bits and each byte = 8 bits. "00" is the F1 report, "02" the F0 report.

Non-shaded area
This area is used according with the report read-out after a report is converted to binary. The 0002 is an example from a report.

2.4.5 VERBOSE REPORTS

The following is an example of a Fault Monitor CPU report in Verbose mode:

TrueTime 56000 Site 01
Automatic Reports **Enabled**
Periodic Reports **Disabled**
Primary Inputs Selected REFA No REFB No REFC Off PRI OK SEC OK TER Off

1. Undefined	OK	Undefined	OK
2. Undefined	OK	Undefined	OK
3. 5201-X	**LOCAL OSC FAULT 0002**	**Undefined**	**OK**
4. Undefined	OK	Undefined	OK

The above sample tells you that:
Automatic reports are enabled and Periodic reports are disabled. Primary inputs REF A and REF B are not buffering Aux. Ref. REF C is OFF. Primary and Secondary status inputs OK, Tertiary is OFF.

Numbers 1-4 are slots (not all slots are shown in the example). Slots 1,2,and 4 are undefined (empty) and functional (OK).

Slot 3 is read as follows:
5201-X is the abbreviation of the 560-5201-X card. The fault reading is 0002.

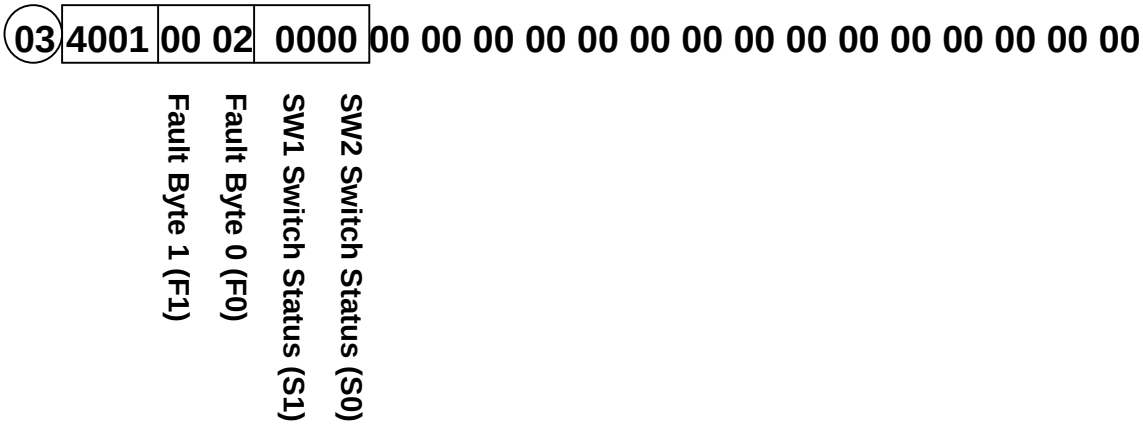
2.4.6 MACHINE REPORTS

The Fault Monitor CPU has another serial output mode called machine report mode. This mode is usually used with a computer program to interrogate the 56000 system status.
The machine report mode displays hexadecimal (HEX) characters like the verbose mode report.

The following is an example of a Fault Monitor CPU report in Machine Mode:

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 40 01 00 02 0000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Example from card slot 3:



Slot 3 shows that the Fault status is 0002 (F1, F0). The Status report read-out is 0000(S1, S0). There is no Status report for this card.

2.4.7 REPORT CONVERSIONS

This section deals with how to read and convert the Fault and Status read-outs using various tables and binary conversions. To decipher a Fault Status report, use Fig. A.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/Switch On
0 = No Fault/Switch Off

Use the Binary Conversion table to convert a read-out from the monitor to binary. For instance, if the report read-out was 3C15, this would be:

11\1100\1\101 in binary.

USING THE FAULT STATUS REPORT (F0, F1)

The hex weight (fault importance) has been assigned 8, 4, 2, 1. Beneath each number is the corresponding fault. Use Fig. A. The report example read 002. The 0 is high byte/high nibble, the 0, high byte/low nibble, the 0, low byte/high nibble and 2, low byte/low nibble. Each nibble falls under a section on Fig. A, high to low or left to right.

Look at Fig. A. Below this is a sample read-out. This read-out would appear on the monitor when a Verbose report is requested. In the example, there are no faults in the upper byte/high nibble or in the lower byte/high nibble because both are zero (0). In the upper byte/low nibble, a 0 is reported also. However, In the lower byte/low nibble a 2 is reported. Use the Binary Conversion table to determine the faults.

Two (2) is converted to 10 in Binary. In Binary, a 1 = fault and 0 = no fault. Read 1,0 from right (low bit) to left (high bit) using the lower byte/low nibble group. The first two (from low bit to high bit) are 0 and 1. There is a fault with the Bus Signal.

Of course, glancing at the low byte/low nibble, you can quickly see (without converting to binary) that under 2 is the Bus fault.

Each of the four nibbles is grouped by category for easy visual identification of an offending fault. Each nibble has 15 possible fault combinations. All faults are asserted as a logic 1.

QUICK REFERENCE SHEET FOR READING FAULT AND STATUS REPORTS

1. Run a report. This is a portion of a sample Machine report.

TrueTime 56000 Site 01
AR1
PR10
P A1 B1 Co P1 S1 To
01 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
03 40 01 00 02 0000 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
04 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
(card slots 05 through 14 HEX not shown)

0002 is the Fault Status read-out
0000 is the Status read-out report

03 4001 00 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00

Fault Byte 1 (F1)
Fault Byte 0 (F0)
SW1 Switch Status (S1)
SW2 Switch Status (S0)

Slot 3 shows that the Fault status is 0002 (F1, F0). The Status report read-out is 0000(S1,S0).

00 = Fault Status 1 (F1) report
02 = Fault Status 0 (F0) report
00 = Status 1 (S1) report
00 = Status 0 (S0) report

What's in a number?

0 4 0 7

High Byte High Nibble — High Byte Low Nibble — Low Byte High Nibble — Low Byte Low Nibble

2. When required, convert Decimal to Binary using the Binary Conversion Table.

BINARY CONVERSION TABLE

Decimal	Displayed in report as	Binary
0	0	0
1	1	1
2	2	10
3	3	11
4	4	100
5	5	101
6	6	110
7	7	111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Binary:
1 = Fault/On/Active
0 = No Fault/Off/Not Active

2.5. MAINTENANCE

Cap unused fiber plugs.

SECTION THREE

3. THEORY OF OPERATION

3.1. GENERAL INFORMATION

This section contains a detailed description of the circuits in the Fiber Optic FM Transceiver card.

3.2. CIRCUIT BOARD DESCRIPTION

The 560-5201-X Assembly provides a single Fiber Optic input channel which may be connected to any one of eight signal bus traces by means of a switch. It also provides a single Fiber Optic output channel which repeats the Fiber Optic for use as a repeater, echoing whatever is fed to the input channel out onto the output channel.

3.3. DETAILED DESCRIPTION

Reference drawing 560-5201-X, sheet 2 of 3

3.3.1. INPUT CHANNEL

The signal comes on board via J2 which is a Fiber Optic Receiver. C23 AC couples and R35 terminates the output of the receiver. L2 and C24 are series resonant at 10 MHz and serves as a Bandpass filter. R36 biases the amplifier chain of U7:A, U7:B, and U7:C into its linear operating region so that they operate as cascaded RF amplifiers. Gain is sufficient to achieve limiting with a 2 KM long fiber. The output of the limiter is sent three places, a phase shift network (consisting of R37, C25, C26, R38, U7:E, and U7D), and inputs of two exclusive OR gates serving as phase detector. The phase shifted signal is applied to the other inputs of the exclusive OR gates, and at the nominal 10 MHz center frequency is 90 degrees out of phase with the other signal. Due to the action of the exclusive OR gates, a 50% duty cycle 20 MHz Squarewave will be seen on their outputs. This signal is integrated over time by R40 and C27 with a long time constant and by R39 and C28 with a short time constant. With no modulation present, both signal will be equal and about midway between the rails. When modulation is present, a signal which follows the modulation will be superimposed on the steady state level of the short TC integrator, but will not be seen on the long TC integrator. This signal is used to re-establish a zero baseline for the output signal in following circuits. It also compensates for frequency drift and other time an temperature effects over a wide range. U10:A and U10:B are voltage followers which buffer the integrators to maximize their tracking ability. U11:B inverts the output of the long TC integrator and applies to a summing node at R52. R1 allows for minor offsets to be removed from the output signal when analog signals are being output and serves as a symmetry adjustment when digital squarewaves are being output. The

short TC signal is fed to the other summing node at R53. U11:A is a non-inverting summing amplifier with a fixed gain of 11. It serves to combine the short TC signal with the inverted long TC signal to produce an AC signal centered around zero volts. Its output is fed to R57 which serves to adjust the output level of U12:B. This is a gain stage with a fixed gain of 11. Its output is fed to U15 if JP1 is in position 1-2 and to the inverting input of comparator U4. If U15 is fed by U12:B then the output will be an analog signal closely replicating the analog signal at the transmitter. If JP1 is in position 2-3 then the output will be a digital replica of the input at the transmitter. It is re-generated by U4 from the analog signal from U12:B compared to a reference of 0 volts generated by U11:A. U11:A may also be configured for other reference voltages. CR3 and CR4 prevent saturation of the comparator and C36 was added to prevent input referred noise from causing hash at the zero transitions of the comparator. U14 was added to square up the edges from the comparator. Note again that in this mode of operation, R1 may be used to adjust the symmetry of a square wave. The U15 output is taken off-board by R82. Note that the output may be terminated with a 50 ohm load without loss in signal amplitude because U15 is easily able to drive plus and minus 300 milliamps.

3.3.1.1. MODE SETTING (RECEIVER END)

The receiver is set up for AM (560-5201-1) or DC (560-5201-2) mode with a single jumper: JP1, which is set to position 1-2 for AM mode and to position 2-3 for DC mode.

3.3.2. OUTPUT CHANNEL

The source of the re-transmitted output is the third stage of the linear amplifier U7:C which directly drives the unity gain power buffer U5. U5 drives the Fiber Output transmitter through the current limiting resister R29. The output activity is sampled at the high current buffer U5 and integrated into a DC component which keeps the comparator U3 in a low output state when there is a signal present on the fiber transmitter input. There are no mode setting for the transmitter as no option has been made to allow sourcing from anywhere other than the input signal.

3.3.3. POWER SUPPLY

Power is applied to the board at a nominal 48 VDC level. It is filtered by L1, C1, D1, and C2, and applied to a DC to DC converter, PS1, which is used to supply $\pm$5 VDC to the on card circuitry. Both the -5 VDC and the +5 VDC levels are heavily filtered by tantalum and ceramic capacitor.

SECTION FOUR

4. DRAWINGS

4.1. 560-5201-X ASSEMBLY DRAWINGS AND BILL OF MATERIALS